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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,038	06/27/2003	Chien-Chung Tseng	MXIC-P910232	8465
7590	05/18/2005			EXAMINER ENGLUND, TERRY LEE
Kenton R. Mullins Stout, Uxa, Buyan & Mullins, LLP Suite 300 4 Venture Irvine, CA 92618			ART UNIT 2816	PAPER NUMBER
DATE MAILED: 05/18/2005				

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/609,038	TSENG ET AL.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) Responsive to communication(s) filed on Amdt/Dwgs (Jan 4) & Dwgs (Mar 3, 2005).
 2a) This action is **FINAL**. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) Claim(s) 1-25 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) 23 and 24 is/are allowed.
 6) Claim(s) 1-5,7,8,10,13-19, 21 and 25 is/are rejected.
 7) Claim(s) 6, 9, 11, 12, 20, and 22 is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on 03 March 2005 is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)	4) <input type="checkbox"/> Interview Summary (PTO-413)
2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)	Paper No(s)/Mail Date. _____.
3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.	5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)
	6) <input type="checkbox"/> Other: _____.

DETAILED ACTION

Response to Amendment/Drawings

The amendment and drawings submitted on Jan 10, 2005, and the drawings submitted on Feb 28, 2005 have been reviewed and considered with the following results:

The Jan 10th drawings were not identified as Replacement Sheets, and therefore were considered non-compliant. However, the drawings submitted on Feb 28, 2005 were correctly labeled, and they overcame the drawing objections described in the previous Office Action. Those objections have now been withdrawn.

The change to page 10 overcame the objection with respect to the reversed “drain” and “source” recitations on lines 9-12. Therefore, that objection has been withdrawn.

The amended claims overcame all the objections to claims 3, 7-8, and 10-22 as described in the previous Office Action. However, when the claims were reviewed, several other objections were noted, and these are described later under the appropriate section.

All but one of the claim rejections under 35 U.S.C. 112, second paragraph described in the previous Office Action were overcome by the amended claims. The rejection of claim 21, with respect to “a reset signal node”, was not addressed/corrected, and it has been maintained. The other previous rejections of claims 1-9 and 14-20 under 35 U.S.C. 112 have now been withdrawn. However, some amended changes, and one newly added claim, have their own respective rejections under 35 U.S.C. 112 as described later under the appropriate section.

The amended claims overcame the various prior art rejections described in the previous Office Action, which have now been withdrawn. Those rejections include: 1) claims 1-2, 4-5, 7-8, and 10 under 35 U.S.C. 102(b) with respect to Smith et al.; 2) claim 10 under 35 U.S.C. 102(e)

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with respect to Slamowitz et al.; 3) claim 3 under 35 U.S.C. 102(b)/103(a) with respect to Smith et al.; and 4) claims 1-5, 7-8, and 14-19 under 35 U.S.C. 103(a) with respect to Slamowitz et al./Smith et al. However, at most of those rejections have been modified to take the amended change(s) into account, and these modified rejections are described later under the appropriate section.

The prior art rejections also include rejections of amended claim 10 with respect to re-interpretation of other prior art references. These rejections are also described later under the appropriate section.

Claim Objections

Claims 6 and 9 are objected to because of the following informalities: For consistent labeling throughout the claims, it is suggested --circuit-- be added after “trigger” on line 4 of claim 6. Claim 9 appears to have two periods at the end of the claim. Therefore, it is suggested one of them be deleted. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

The phrases “relatively small” and “relatively large” in claims 2 and 4, respectively uses relative terms which render the claim indefinite. The terms “relatively”, “small”, and “large” are not defined by the claim, the specification does not provide a standard for ascertaining the requisite degree, and one of ordinary skill in the art would not be reasonably apprised of the scope of the invention. For example, is the pulse (or resistor) related to the size of another pulse (or resistor) within the same circuit? Also, what is actually considered to be “relatively small” or

“relatively large”? Claims 15 and 17 have the same “relatively small” and “relatively large” problem as claims 2 and 4, respectively.

Claim 13 recites the limitation “the decrease in the primary current” in lines 5-6. There is insufficient antecedent basis for this limitation in the claim.

Claim 21 remains rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. It is not clear how “a reset signal node” on line 2 of claim 21 relates to the “reset signal node” recited within claim 20. For example, are they the same node, or two distinct signal nodes? Related to this node (or nodes), since claim 20 implies the reset signal node can rise from a ground potential to a first voltage in response to the supply signal during a power-down mode, how can the same node rise to a second voltage during the power-down mode as lines 4-5 of claim 21 recites?

Claim 25 recites the limitation “the decrease in the primary current” in lines 5-6 with insufficient antecedent basis for this limitation in the claim, or its chain of dependency.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-2, 4-5, and 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith et al. (Smith), a reference cited in the previous Office Action. Fig. 3 shows a power-on reset circuit comprising Schmitt trigger circuit 46 and voltage divider 51,50,44 connected to

input 52 of Schmitt trigger circuit 46. Fig. 8 shows an example of Schmitt trigger circuit 46 comprising a plurality of MOS devices (e.g. M20-M24,H25; M20-M21,M24; and/or M22-M23,H25), wherein the reference does not indicate the MOS devices have different threshold values. Therefore, each device is considered as having the same threshold V_t (e.g. within acceptable fabrication tolerances). From the circuitry and waveforms shown in the figures, one of ordinary skill in the art would understand the devices determine the power reset trigger level. Using Fig 10 as a reference, reset signal 88 transitions from a low to high level once the power supply (represented by the solid “86,88” line) has reached a power-up threshold greater than midpoint 92 of the nominal power supply voltage range, and reset signal 88 transitions from a high to a low level once the power supply has decreased below a power-down threshold that is less than midpoint 92 (e.g. see column 10, lines 28-43). Section 51 of voltage divider 51,50,44 provides signals trgrdn and trgrup, which track (e.g. are proportional to) supply signal VDD (e.g. see columns 6 (lines 38-41) and 7 (lines 710)). Therefore, claim 1 is anticipated. Fig. 4 shows a temperature and voltage compensated reference generator circuit 62 (e.g. see column 7, lines 47-51) that provides its signal vref to voltage divider section 44, and it is operatively coupled to Schmitt trigger circuit 46. Deeming the Fig. 4 circuit as a compensate circuit that generates a “relatively small reset pulse” (e.g. the reference voltage) that compensates for temperature and supply signal variations, claim 2 is anticipated. Low-side resistor R5 is larger than resistor R4 (e.g. see column 7, lines 21-22), and this relatively larger size can help reduce any leakage (e.g. unnecessary) current, thus anticipating claim 4. When the compensate circuit of Fig. 4 is considered to be part of the voltage divider, it effectively adjusts a feedback current (e.g. via 54, 50, 60, and 52) to help restore (e.g. maintain) voltage pupdn at input 52 of Schmitt trigger circuit

46, and claim 5 is anticipated. Referring to Figs. 3 and 11, Schmitt trigger circuit 46 has reset signal node 54 that provides a reset signal 88 (e.g. pwrenb) that rises from ground potential (e.g. a logic low) to a first voltage (e.g. a logic high) when supply signal 86 has increased enough to favorably compare to a first threshold voltage 96 (e.g. signal 86 > voltage 96); and reset signal node 54 drops from the first voltage to the ground potential when supply signal 86 does not compare favorably to the first threshold voltage 96 (e.g. voltage 98 < voltage 96). Since the Smith reference does not clearly show or disclose a sleep mode, one of ordinary skill in the art could consider Smith's power-on reset circuit' operation corresponds to the normal operation of a power-on reset circuit that includes power-up and power-down modes, but does not include a sleep mode. Without a sleep mode, the circuit does not enter into it, and claim 7 is anticipated. Interpreting Fig. 11 in a slightly different manner, and also referring to Fig. 10, one of ordinary skill in the art would understand Schmitt trigger circuit 46 has a first voltage peak (e.g. 98 of Fig. 11 corresponds to the power-down threshold level shown in Fig. 10 that is represented by the intersection of lines 88 and 86 shown below 92), and a second voltage peak (e.g. 96 of Fig. 11 corresponds to the power-up threshold level shown in Fig. 10 that is represented by the intersection of lines 86 and 88 shown above 92). Since 98 corresponds to when Schmitt trigger circuit 46 enters a power-down mode, and 96 corresponds to when Schmitt trigger circuit 46 exits the power-down mode (e.g. returns to a normal, active operation), claim 8 is anticipated because second voltage peak 96 is greater than first voltage peak 98.

Claim 10 is rejected under 35 U.S.C. 102(b) as being anticipated by Savignac et al. (Savignac), a reference reviewed during a recent update search. Fig. 2 shows a reset circuit one of ordinary skill in the art would understand relates to a method for providing a reset signal in

response to a supply signal. The method comprises generating a primary current (through T4,T5,D) in response to supply signal VDDx; generating trigger voltage VB (and/or VC) in response to the primary current; if the sleep mode has not been entered (e.g. the circuit is operating during the normal power up sequence) and supply signal has not compared favorably to a first threshold level (e.g. has not reached the trigger point of I1 (and/or I2)), reset signal VD increases from reference potential VSS to a first potential (see VD at point t4 shown in Fig. 3) in response to an increase in supply signal VDDx; and once supply signal VDDx has compared favorably to the first threshold level, reset signal VD is set to reference potential VSS (e.g. see the waveforms shown in Fig. 3). At this time, the circuit can be considered as having effectively entered a sleep mode because the power-up sequence has been completed, and reset signal VD will remain at reference potential VSS until the power-up sequence is again required. Therefore, claim 10 is anticipated.

Claim 10 is also rejected under 35 U.S.C. 102(b) as being anticipated by Giovinazzi et al. (Giovinazzi), another reference reconsidered during the recent update search. Fig. 2 shows a reset circuit one of ordinary skill in the art would understand relates to a method for providing a reset signal in response to a supply signal. The method comprises generating a primary current (through 1,2,T2) in response to supply signal Vdd; generating trigger voltage Sd in response to the primary current; if the sleep mode has not been entered (e.g. the circuit is operating during the normal power up sequence) and supply signal Vdd has not compared favorably to a first threshold level (e.g. has not reached the trigger point of 3), reset signal POR increases from a reference potential to a first potential (see Fig. 1) in response to an increase in supply signal Vdd; and once supply signal Vdd has compared favorably to the first threshold level, reset signal POR

is set to the reference potential (e.g. see the waveforms shown in Fig. 1). At this time, the circuit can be considered as having effectively entered a sleep mode because the power-up sequence has been completed, and reset signal POR will effectively remain at the reference potential until the power-up sequence is again required. Therefore, claim 10 is anticipated.

Claim Rejections - 35 USC § 102/103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 102(b) as anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Smith et al. (Smith) as applied to claim 1 above. As previously described, Smith shows a power-on reset circuit comprising Schmitt trigger circuit 46 and voltage divider 51,50,44. Voltage divider section 44 is shown in Fig. 7 comprising current source transistors M15 and M18 which will generate current in response to the supply signal, thus anticipating claim 3. However, voltage divider section 51 can be modified to include a current source transistor. For example, it would have been obvious to one of ordinary skill in the art to replace at least one of resistors R3-R5 with a corresponding transistor receiving a respective bias voltage to control its resistance. Each transistor can be deemed a current source transistor that will generate current (e.g. allow current to flow through it) in response to the supply signal, thus rendering claim 3 obvious. By replacing at least one of resistors R3-R5 with a transistor, the trigger voltages trgrdn and trgrup can be adjusted to desired levels. For example, perhaps the power-up level is not what was initially expected. Therefore, if voltage divider

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section 51 has at least one (current source) transistor within its current path, the power-up level can be adjusted by changing the bias voltage to the transistor(s) to meet a required level. The more resistors that are replaced by a corresponding transistor, the more accurate the trigger levels can be set after fabrication.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-5, 7-8, and 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slamowitz et al. (Slamowitz), in view of Smith et al. (Smith), wherein both of these references had been cited in the previous Office Action. Fig. 4 of Slamowitz shows a power-on reset circuit comprising Schmitt trigger circuit 442 for determining a power reset trigger level of signal schmit_out; and voltage divider circuit 410,412 is connected to the input of Schmitt trigger circuit 442. As shown in Fig. 5, and understood by one of ordinary skill in the art,

voltage divider section 412 tracks supply signal Vddc. However, the reference of Slamowitz does not show or disclose Schmitt trigger circuit 442 constructed with a plurality of MOS devices, or wherein the power-on reset circuit is within a computer system that comprises a microprocessor, bus, and memory. Fig. 8 of Smith shows Schmitt trigger circuit 46 comprising a plurality of MOS devices (e.g. M20-M24,H25; M20-M21,M24; and/or M22-M23,H25). Therefore, it would have been obvious to one of ordinary skill in the art to replace Slamowitz's Schmitt trigger circuit 442 with Smith's Schmitt trigger circuit 46. Since Smith does not indicate the threshold voltages of the MOS devices are different from one another, they are considered as having the same threshold V_t (e.g. within acceptable fabrication tolerances). One of ordinary skill in the art knows a Schmitt trigger has a power-up threshold higher than its power-down threshold, with respect to the power reset trigger level, the Slamowitz/Smith configuration renders claim 1 obvious. The use of Smith's Schmitt trigger circuit simply replaces the generic Schmitt trigger circuit of Slamowitz (e.g. details of that circuit is not shown/disclosed) with one specific, known Schmitt trigger circuit. Slamowitz's 438 can be considered one type of a compensate circuit that compensates for temperature and supply signal variations (e.g. see paragraph 0042, wherein it is understood that changes in temperature can also affect and/or cause power supply type changes). The on/off operation of 438 will generate what can be deemed a "relatively small reset pulse", and since it is operatively coupled to the Schmitt trigger circuit, claim 2 is rendered obvious. Voltage divider section 412 includes current source transistors 434 and 414, which generate a current in response to supply signal vddc, and claim 3 is rendered obvious. Referring to a resistor divider circuit, paragraphs 0012 and 0039 both indicate the series resistors can have different resistance values. Therefore, when resistors 416 and 418 are

of different values, the large one can be considered a “relatively large low-side resistor” (e.g. both resistors are coupled between 414 and low side gnnd). Since both resistors limit the current flowing through the series path of 434,414,416,418, each one effectively reduces leakage (e.g. unnecessary) current, rendering claim 4 obvious. Transistor 438, included in voltage divider 410,412, provides one type of compensate circuit that adjusts a feedback current to help restore (e.g. maintain) the voltage at the input of Schmitt trigger circuit 442 in response to supply signal fluctuations (e.g. see paragraph 0042, wherein one of ordinary skill in the art would understand the phrase “prevent false re-triggering” is one way of stating the signal is not changed enough to cause inaccurate triggering of the power-on reset circuit). Therefore, claim 5 is rendered obvious. Since the Slamowitz/Smith configuration is understood to operate as a power-on reset circuit with power-up and power-down modes, it will not enter a sleep mode. Therefore, one of ordinary skill in the art will understand that the Schmitt trigger circuit will comprise a reset signal node that has a signal that will rise from a ground potential (e.g. a logic low) to a first voltage (e.g. a logic high) as the supply signal increases and it compares favorably with a first threshold voltage (e.g. it’s equal to, or greater than, the power-up threshold). Also, the signal at the reset signal node will drop from the first voltage to the ground potential when the supply signal does not compare favorably to the first threshold voltage (e.g. it’s below the first threshold voltage by a predetermined amount), thus rendering claim 7 obvious. Understanding the operation of a Schmitt trigger circuit, one of ordinary skill in the art will understand that the signal on a reset signal node has a first voltage peak (e.g. power-down threshold level) when the Schmitt trigger circuit enters a power-down mode, and a second voltage peak (e.g. power-up threshold level), greater than the first voltage peak, when the Schmitt trigger circuit exits the

power-down mode (e.g. enters the active mode). Therefore, claim 8 is rendered obvious. It also would have been obvious to one of ordinary skill in the art to use the Slamowitz/Smith power-on reset circuit within a computer system comprising a microprocessor coupled to a memory by a bus, wherein the power-on reset circuit would generate a power-on reset signal to the microprocessor. Computer systems typically comprise some type of a power-on reset circuit to ensure the power supply circuit has reached at least a minimum acceptable voltage level that will ensure the system will operate properly. This use is considered one known and intended use for a power-on reset circuit by the examiner. By letting the computer's processor know when the power supply is within, or below, its acceptable limits, the power-on reset circuit can minimize inaccurate operations of the computer system. Other than the additional computer system, microprocessor, bus, and memory limitations recited within independent claim 14, the power-on reset circuit limitations of claims 14-17 and 19 correspond to the limitations recited in claims 1-4 and 7, respectively. Therefore, claims 14-17 and 19 are rendered obvious for the same reasons as described above with respect to the rejections of claims 1-4 and 7. Although claim 18 closely corresponds to claim 5, claim 18 recites "in response to a fluctuation in temperature", wherein claim 5 recites "in response to a fluctuation in the supply signal." However, it would have been obvious to one of ordinary skill in the art to consider that 438 can function as one type of a compensate circuit that adjusts feedback current in response to temperature fluctuations, because it is understood that changes in temperature can also affect supply signal levels. Since 438 provides hysteresis to help prevent false re-triggering in the presence of power supply fluctuations (e.g. see paragraph 0042), 438 can also help compensate for temperature fluctuations that affect the power supply. Therefore, claim 18 is rendered obvious.

Allowable Subject Matter

Claims 23-24 are allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the method for providing a reset signal includes the specific relationships between the sleep mode, power-up state, power-down state, and first/second potential as recited within claim 23, upon which claim depends.

Claims 6, 9, 11-12, 20, and 22 are only objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no motivation to modify or combine any prior art reference(s) to ensure: 1) a threshold-enhancement node has the first/second voltages with respect to the power-down and sleep modes as recited within claim 6; 2) the reset node has a third voltage when the sleep mode is entered and exited as recited within claim 9; 3) the method steps also include the increase to the first/second potentials in response to the supply signal when a power-up/power-down state is respectively entered as recited within claim 11, upon which claims 12-13 depend; 4) the specific relationships with respect to the rising of the first voltage and the power-up, power-down, and sleep modes as recited within claim 20; and 5) the rising of the first/second voltages with respect to the power-up/power-down modes as recited within claim 22.

Also, claims 13, 21 and 25 would be allowable if rewritten to satisfactorily overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. These claims depend on objected to claims 11 and 20, and allowed claim 23, respectively.

Response to Comments

Page 10 of the amendment refers to amended claims 1 and 14, as well as to the last (full) paragraphs on pages 2 and 15 of the applicants' specification. The claims had the phrase "each of said devices having the same" added prior to V_t; page 2 indicates "all of the transistors have a uniform threshold voltage", and page 15 cites "a plurality of MOS devices of one V_t." However, what is considered a plurality of MOS devices having the same V_t (i.e. threshold) is never clearly defined. Using the Schmitt trigger circuit of Smith's Fig. 8 as an example, one of ordinary skill in the art will see the circuit is shown with a total of six MOS devices. This plurality of six devices in itself comprises a plurality of three PMOS devices (i.e. M20-M21, and M24), and a plurality of three NMOS devices (i.e. M22-M23, and H25). Therefore, any one of these pluralities, or any two of the devices, can be considered a plurality of MOS devices. Unless a reference clearly shows or discloses differences in sizes and/or thresholds, devices within a reference are considered to have the same characteristics. Even if there is a possible difference in threshold values between PMOS and NMOS devices, the difference between devices of the same conductivity type will be minimal (e.g. within acceptable fabrication tolerances), and thus they would be considered to have the same threshold V_t as one another.

Therefore, the rejections described within this Office Action are deemed proper with respect to the broadest interpretation of the claimed limitations, prior art references, and knowledge of one of ordinary skill in the art.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

T.L.E
Terry L. Englund
13 May 2005


TUAN T. LAM
PRIMARY EXAMINER

Proposed Amendments to the Drawings

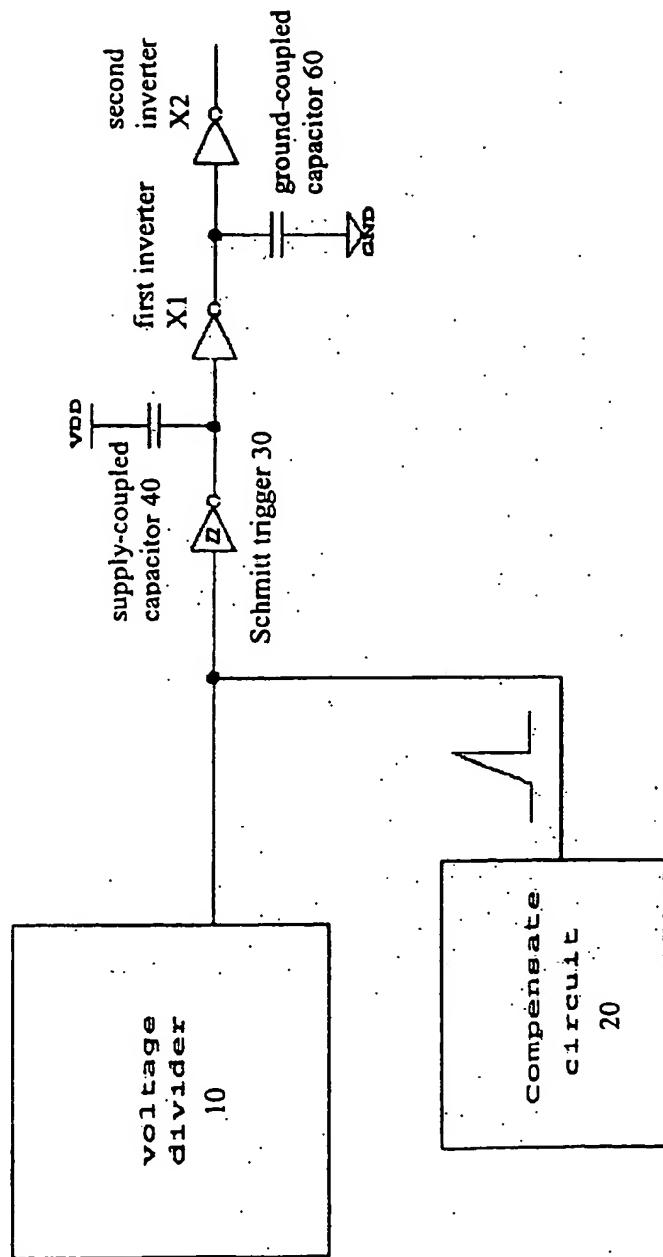
Please see the attached proposed drawing changes as Appendix A.

Drawings submitted
on Jan 9, 2005
not approved - lacked
"Replacement Sheet" label
5.13.05
JZ

Replacement Sheets



Approved
5.13.05
TLE



Replacement Sheets

Approved
5.13.05
TLE

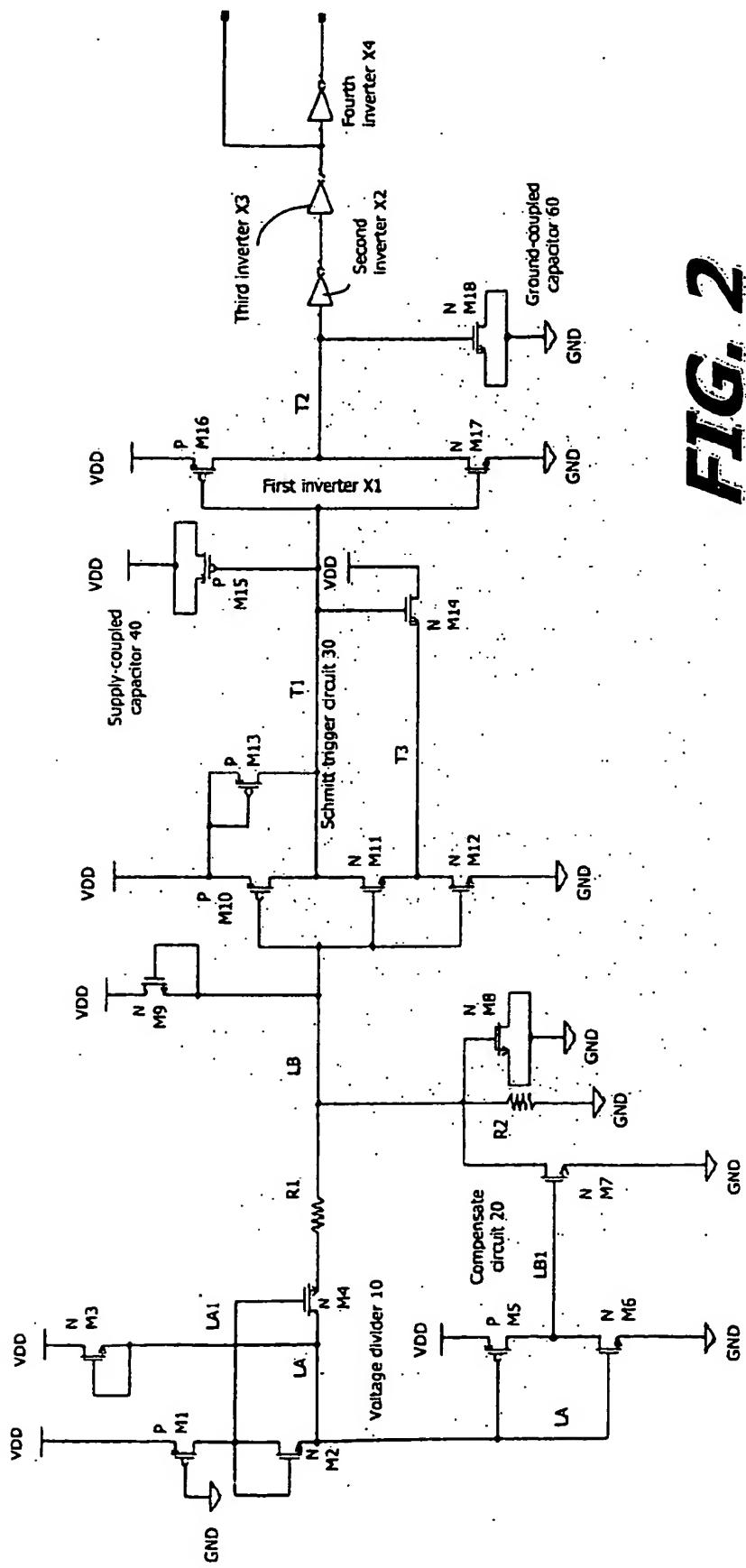


FIG. 2

Replacement Sheets

Approved
5.13.05
TLE

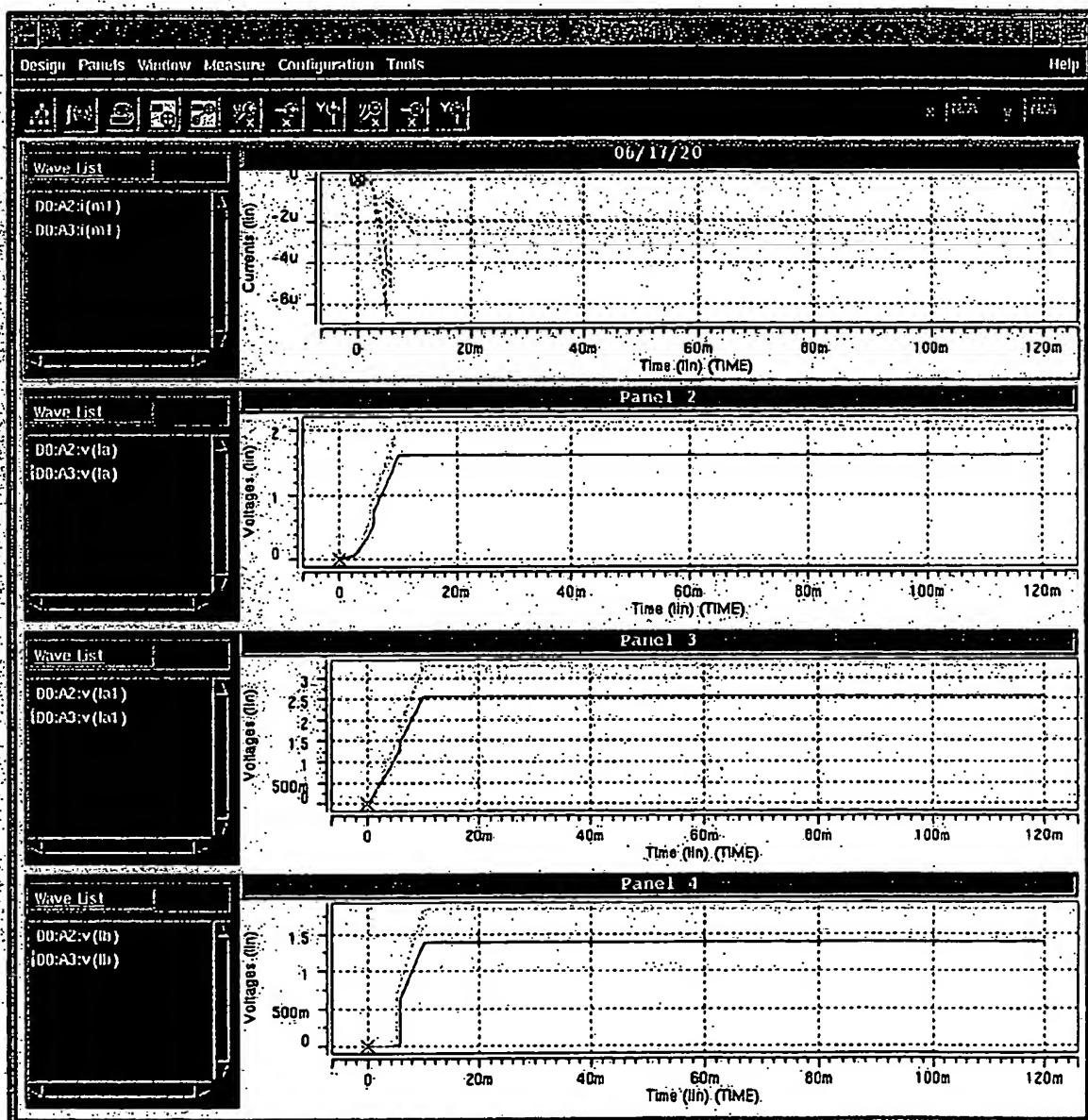


FIG. 3

Replacement Sheets

Approved
5.13.05
1.VE

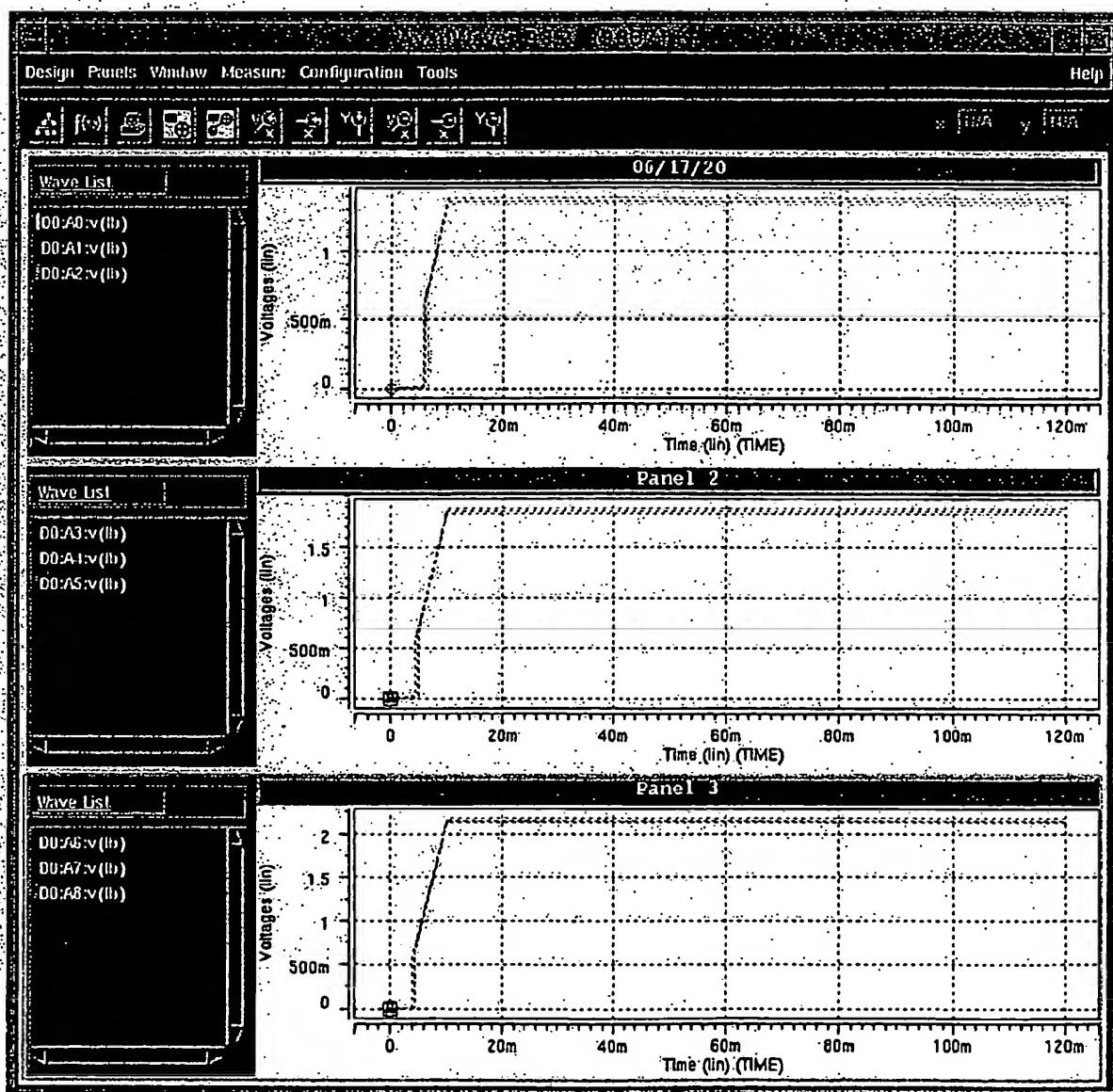


FIG. 4

Replacement Sheets

APR 2003
5.13.05
TKE

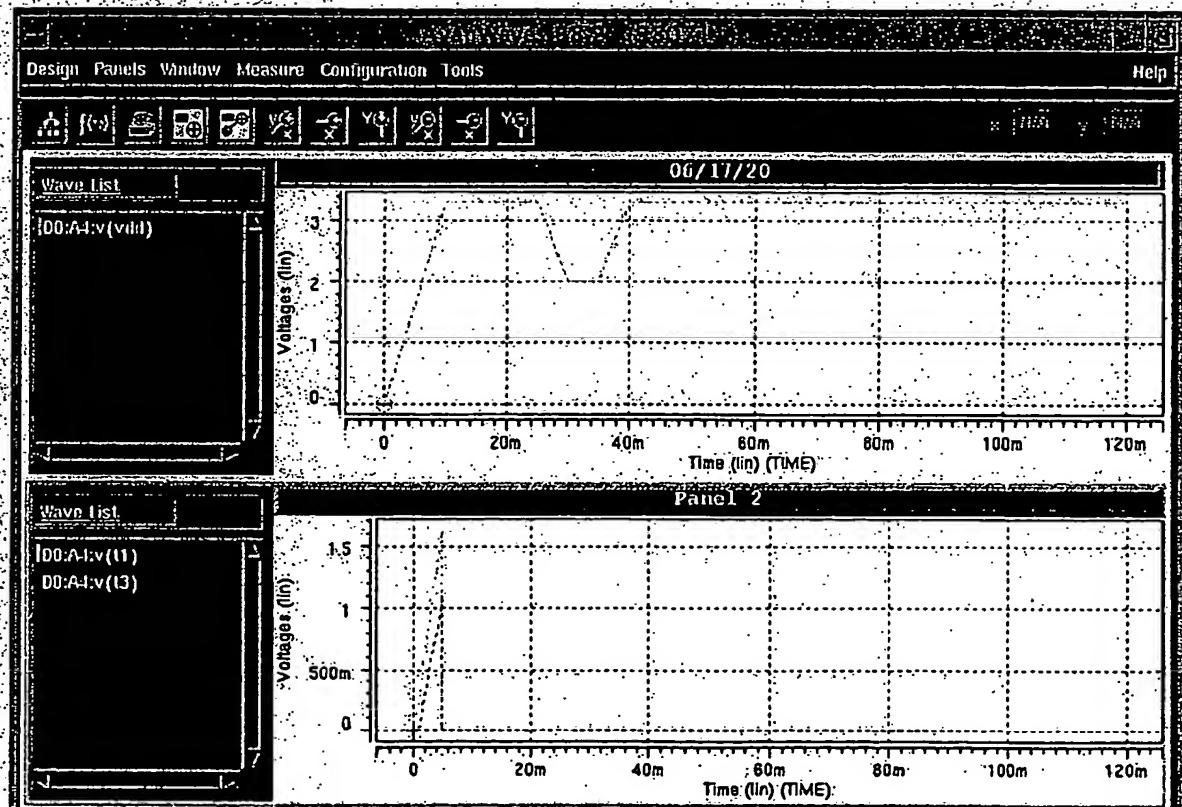


FIG. 5

Replacement Sheets

Approved
5.13.05
TLE

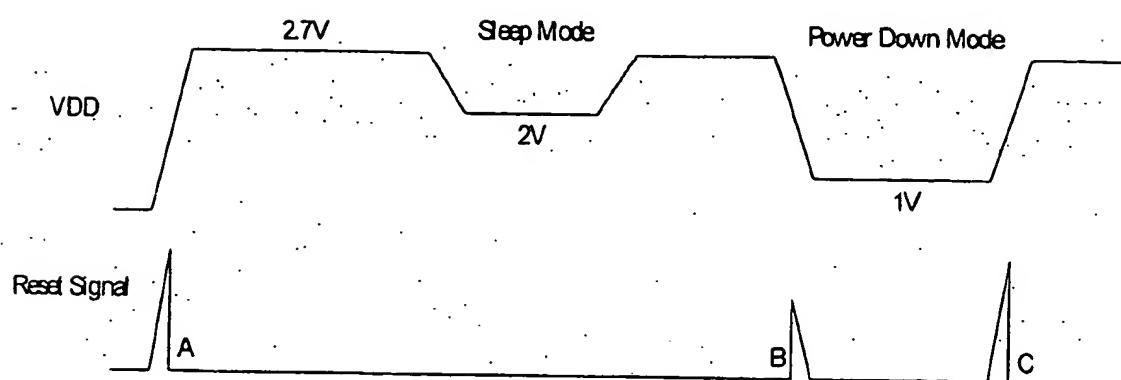


FIG. 6

Replacement Sheets

Approved
6.13.05
TCE

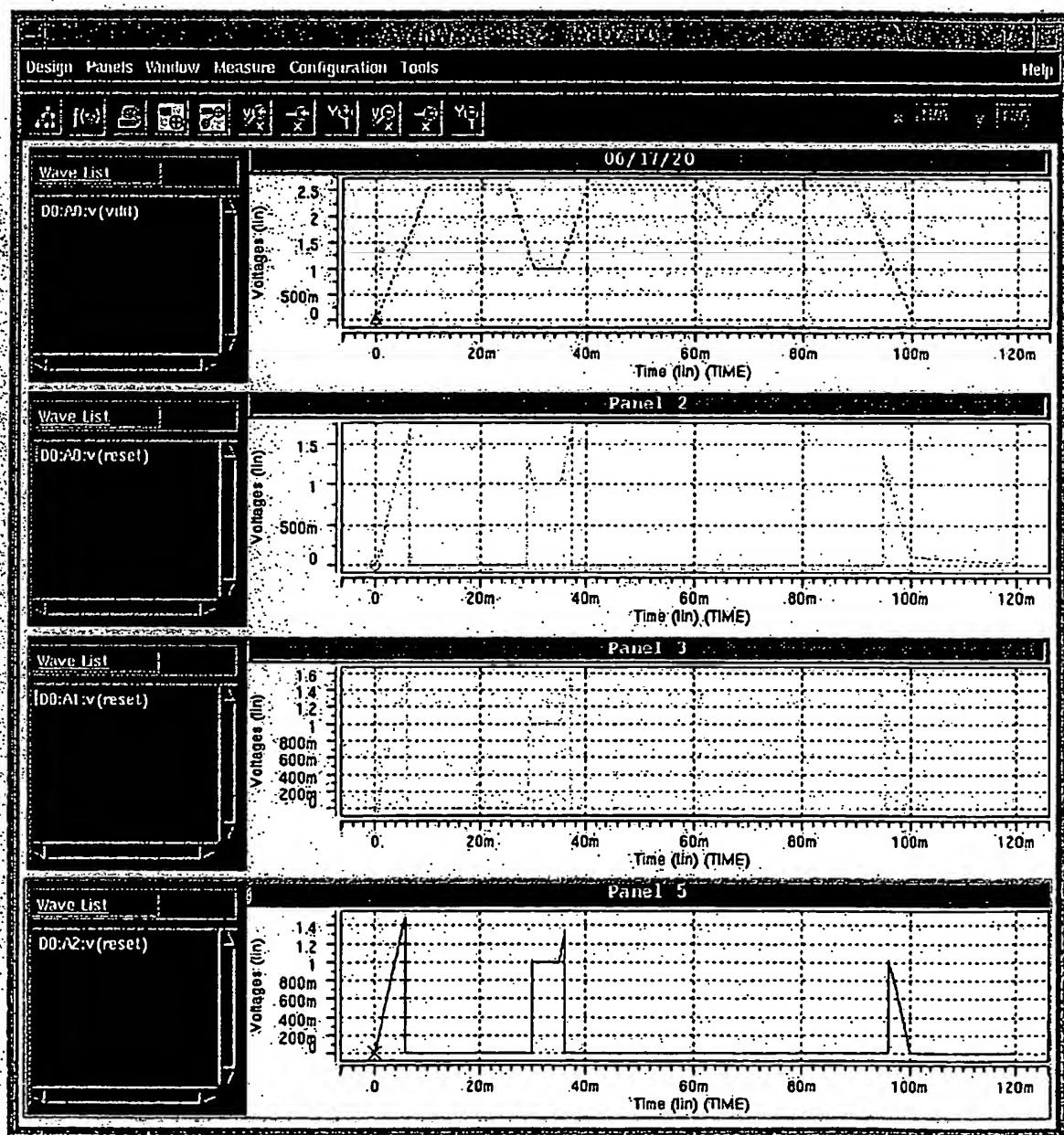


FIG. 7A

Replacement Sheets

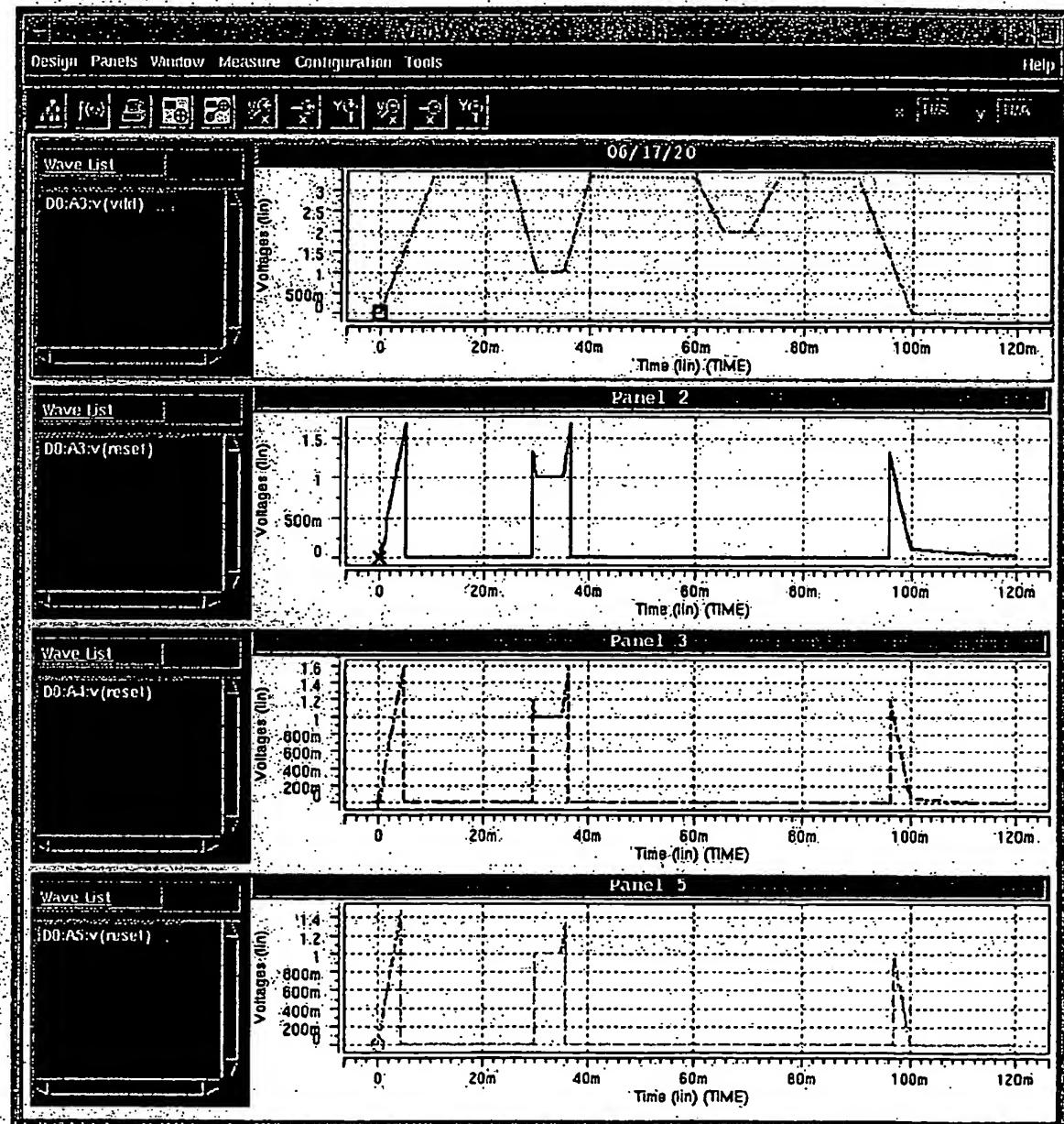


FIG. 7B

Replacement Sheets

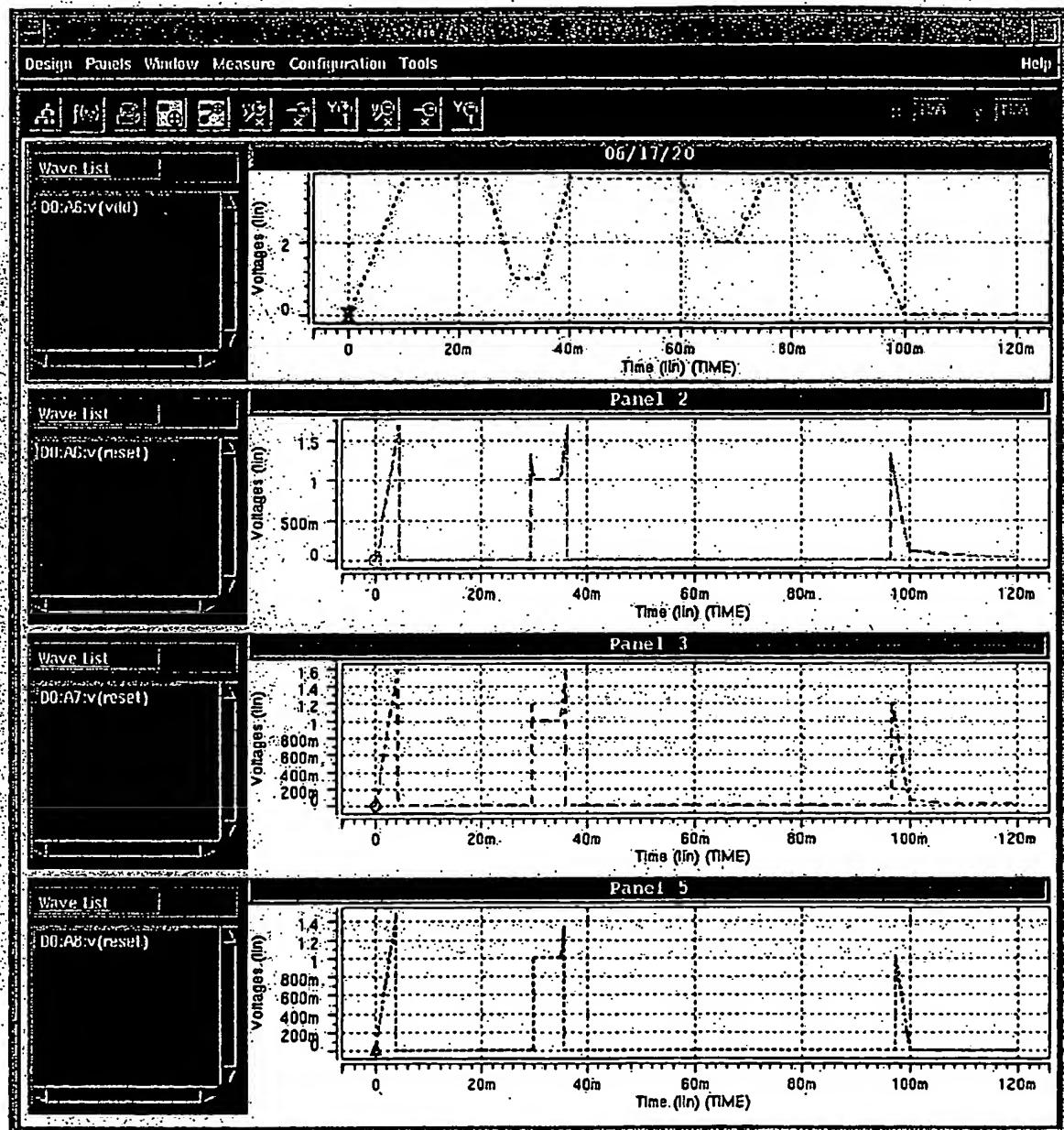


FIG. 7C

Replacement Sheets

Approved
5.13.05
TLE

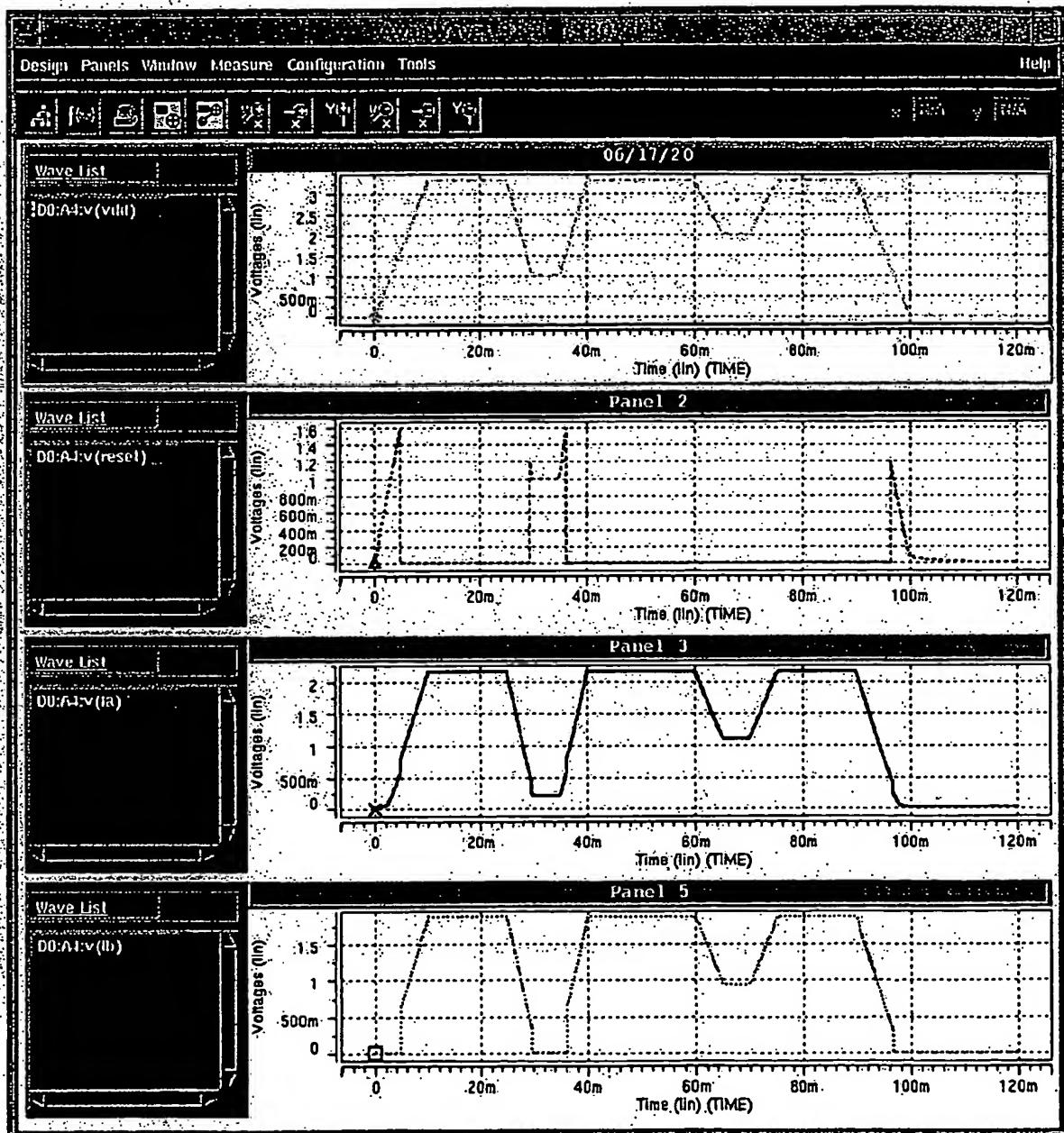


FIG. 8A

Replacement Sheets

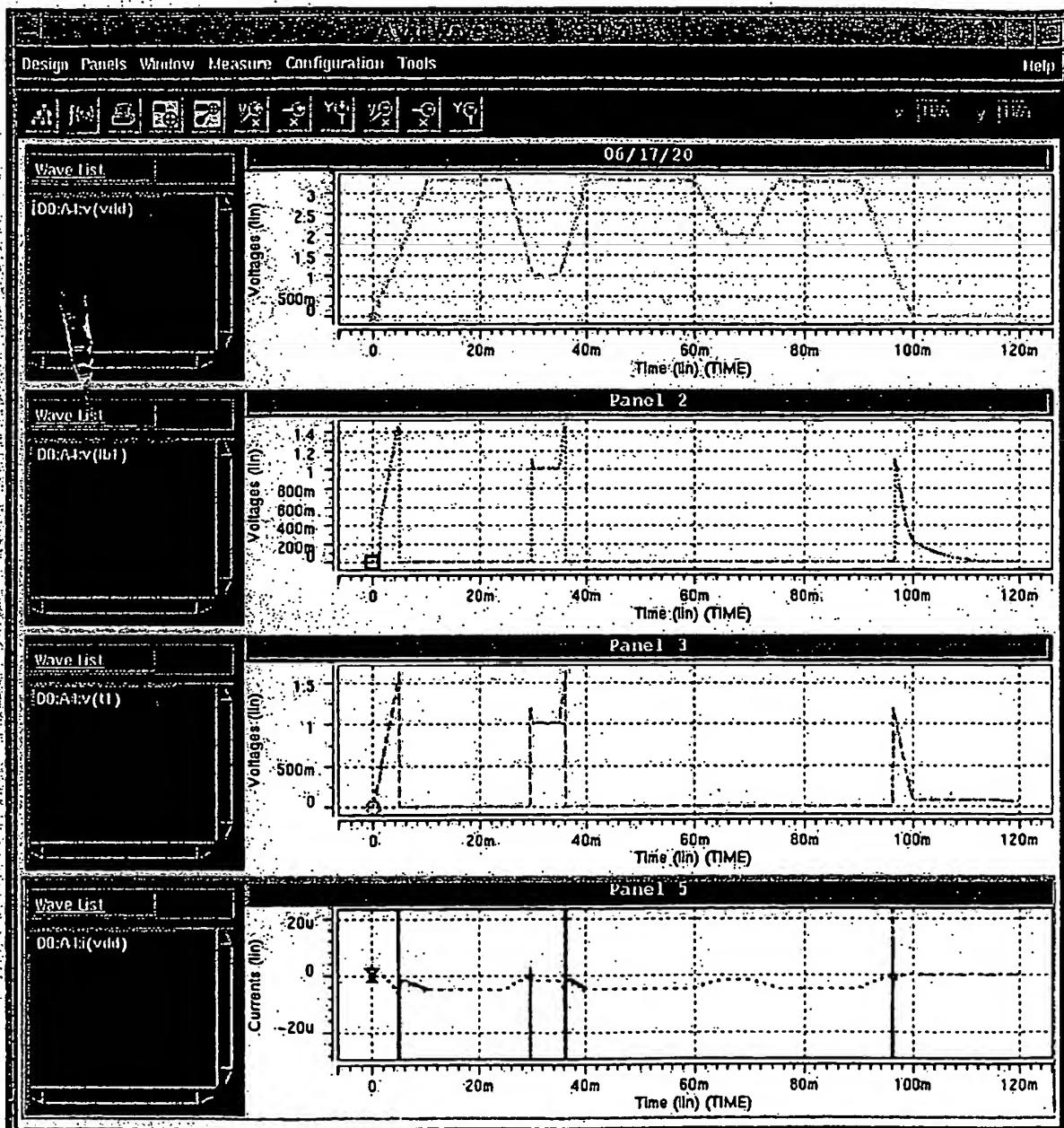


FIG. 8B